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OCT 17 2006

Amendments to the Claims:**Status of Claims:**

Claims 1-30 are pending for examination.

Claims 4-6, 15, 17-20, and 24 are amended herein.

Claims 13, 27, and 28 are cancelled herein.

Claims 1, 4-6, 12, 14-15, 17, 19, 20, 22, 23, 24, 29, and 30 are in independent form.

1. (Original) A correlating debugger, comprising:

a first logic configured to receive a first data set from a hardware analyzer that is configurable to analyze a hardware device;

a second logic configured to receive a second data set from a software analyzer that is configurable to analyze a software component;

a third logic configured to receive a binding data from the hardware analyzer or the software analyzer, where the binding data facilitates synchronizing the first data set and the second data set; and

a fourth logic operably connected to the first logic and the second logic, the fourth logic being configured to:

receive a signal that indicates that an interaction between the hardware device and the software component has occurred; and

upon receiving the signal, to selectively store elements of the first data set and the second data set in a time-ordered data set.

2. (Original) The correlating debugger of claim 1, where the first data set includes one or more of, timing information, state information, state change information, interrupt information, a register value, a memory location value, and voltage information.

3. (Original) The correlating debugger of claim 1, where the second data set includes one or more of, timing information, state information, state change information, interrupt information, a register value, a memory location value, a value for a data variable,

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information about a function call, information about a subroutine call, information about a method call, information about a stack, information about a heap, and information about a procedure call.

4. (Currently Amended) ~~The correlating debugger of claim 1,~~

A correlating debugger, comprising:

a first logic configured to receive a first data set from a hardware analyzer that is configurable to analyze a hardware device;

a second logic configured to receive a second data set from a software analyzer that is configurable to analyze a software component;

a third logic configured to receive a binding data from the hardware analyzer or the software analyzer, where the binding data facilitates synchronizing the first data set and the second data set; and

a fourth logic operably connected to the first logic and the second logic, the fourth logic being configured to:

receive a signal that indicates that an interaction between the hardware device and the software component has occurred; and

upon receiving the signal, to selectively store elements of the first data set and the second data set in a time-ordered data set,

where the hardware device comprises one of, a Universal Serial Bus (USB) device, a Small Computer Systems Interface (SCSI) device, an Industrial Standard Architecture (ISA) device, an Extended Industrial Standard Architecture (EISA) device, a Peripheral Component Interconnect (PCI) device, a PCI Express (PCIE) device, a Serial Advanced Technology Attachment (SATA) device, an Infiniband device, an Ethernet device, a 1394 device, and a Microchannel Architecture (MSA) device.

5. (Currently Amended) ~~The correlating debugger of claim 1,~~

A correlating debugger, comprising:

a first logic configured to receive a first data set from a hardware analyzer that is configurable to analyze a hardware device;

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a second logic configured to receive a second data set from a software analyzer that is configurable to analyze a software component;

a third logic configured to receive a binding data from the hardware analyzer or the software analyzer, where the binding data facilitates synchronizing the first data set and the second data set; and

a fourth logic operably connected to the first logic and the second logic, the fourth logic being configured to:

receive a signal that indicates that an interaction between the hardware device and the software component has occurred; and
upon receiving the signal, to selectively store elements of the first data set and the second data set in a time-ordered data set,

where the software component comprises one of, a device driver, and an application.

6. (Currently Amended) ~~The correlating debugger of claim 1,~~

A correlating debugger, comprising:

a first logic configured to receive a first data set from a hardware analyzer that is configurable to analyze a hardware device;

a second logic configured to receive a second data set from a software analyzer that is configurable to analyze a software component;

a third logic configured to receive a binding data from the hardware analyzer or the software analyzer, where the binding data facilitates synchronizing the first data set and the second data set; and

a fourth logic operably connected to the first logic and the second logic, the fourth logic being configured to:

receive a signal that indicates that an interaction between the hardware device and the software component has occurred; and
upon receiving the signal, to selectively store elements of the first data set and the second data set in a time-ordered data set,

where the binding data comprises a hardware identifier.

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7. (Original) The correlating debugger of claim 1, where the signal comprises a non-maskable interrupt.
8. (Original) The correlating debugger of claim 1, where the time-ordered data set includes one or more first elements of the first data set and one or more second elements of the second data set, where the first elements are arranged together with the second elements in order based on time.
9. (Original) The correlating debugger of claim 1, where the software component is configured to run on a first processor and a processor executable instructions associated with the first logic, the second logic, the third logic, or the fourth logic are configured to run on a second processor.
10. (Original) The correlating debugger of claim 1, where the software component and processor executable instructions associated with one or more of, the first logic, the second logic, the third logic, and the fourth logic are configured to run on a first processor.
11. (Original) The correlating debugger of claim 1, where the software analyzer comprises a kernel debugger.
12. (Original) A system, comprising:
- a first logic configured to receive a first data set from a hardware analyzer that is configurable to analyze a USB hardware device, where the first data set includes one or more of, timing information, state information, state change information, interrupt information, a register value, a memory location value, and voltage information;
 - a second logic configured to receive a second data set from a software analyzer that is configurable to analyze a device driver, where the second data set includes one or more of, timing information, state information, state change information, interrupt information, a register value, a memory location value, a value for a data variable, information about a

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function call, information about a subroutine call, information about a method call, information about a stack, information about a heap, and information about a procedure call;

a third logic configured to receive a hardware identification number from the software analyzer or the software component, where the hardware identification number facilitates synchronizing the first data set with the second data set; and

a fourth logic operably connected to the first logic and the second logic, the fourth logic being configured:

to receive a non-maskable interrupt from the hardware analyzer that indicates that an interaction between the USB hardware device and the device driver has occurred; and

upon receiving the non-maskable interrupt, to selectively store the first data set and elements of the second data set together, in a time-ordered data set.

13. (Cancelled)

14. (Original) A method, comprising:

establishing a relationship in a debugger between a hardware device and a software component that will perform a software operation related to the hardware device;

configuring a software analyzer to collect a first data set related to the software component as the software component performs the software operation and to cause the first data set to be delivered to the debugger;

configuring a hardware analyzer to collect a second data set related to the hardware device as the hardware device performs a hardware operation and to cause the second data set to be delivered to the debugger;

detecting a first event that signals a beginning of the software operation and controlling the software analyzer to begin delivering the first data set to the debugger;

detecting a second event that signals a beginning of the hardware operation and controlling the hardware analyzer to begin delivering the second data set to the debugger; and

selectively storing together, in order, elements of the first data set and elements of the second data set, where the order is based, at least in part, on the time at which an event associated with generating an element occurred.

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15. (Currently Amended) — ~~The method of claim 14,~~

A method, comprising:

establishing a relationship in a debugger between a hardware device and a software component that will perform a software operation related to the hardware device;

configuring a software analyzer to collect a first data set related to the software component as the software component performs the software operation and to cause the first data set to be delivered to the debugger;

configuring a hardware analyzer to collect a second data set related to the hardware device as the hardware device performs a hardware operation and to cause the second data set to be delivered to the debugger;

detecting a first event that signals a beginning of the software operation and controlling the software analyzer to begin delivering the first data set to the debugger;

detecting a second event that signals a beginning of the hardware operation and controlling the hardware analyzer to begin delivering the second data set to the debugger; and

selectively storing together, in order, elements of the first data set and elements of the second data set, where the order is based, at least in part, on the time at which an event associated with generating an element occurred,

where establishing the relationship includes:

identifying a hardware number known to the software component;

communicating the hardware number to the hardware analyzer;

correlating the software component and a hardware device based on the hardware number; and

configuring the hardware analyzer to analyze the hardware device.

16. (Original) The method of claim 15, where the hardware number is based on an I/O request packet (IRP).

17. (Currently Amended) ~~The method of claim 14,~~

A method, comprising:

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establishing a relationship in a debugger between a hardware device and a software component that will perform a software operation related to the hardware device;

configuring a software analyzer to collect a first data set related to the software component as the software component performs the software operation and to cause the first data set to be delivered to the debugger;

configuring a hardware analyzer to collect a second data set related to the hardware device as the hardware device performs a hardware operation and to cause the second data set to be delivered to the debugger;

detecting a first event that signals a beginning of the software operation and controlling the software analyzer to begin delivering the first data set to the debugger;

detecting a second event that signals a beginning of the hardware operation and controlling the hardware analyzer to begin delivering the second data set to the debugger; and

selectively storing together, in order, elements of the first data set and elements of the second data set, where the order is based, at least in part, on the time at which an event associated with generating an element occurred.

where configuring the software analyzer includes one or more of:

identifying one or more types of data available in the software component to be reported on by the software analyzer; and

establishing a frequency with which the one or more types of data will be sampled.

18. (Currently Amended) The method of claim 14, where configuring the hardware analyzer includes one or more of, identifying one or more types of data available in the hardware device to be reported on by the hardware analyzer, and identifying one or more types of events from the hardware device to be reported on by the hardware analyzer.

19. (Currently Amended) ~~The method of claim 14,~~

A method, comprising:

establishing a relationship in a debugger between a hardware device and a software component that will perform a software operation related to the hardware device;

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configuring a software analyzer to collect a first data set related to the software component as the software component performs the software operation and to cause the first data set to be delivered to the debugger;

configuring a hardware analyzer to collect a second data set related to the hardware device as the hardware device performs a hardware operation and to cause the second data set to be delivered to the debugger;

detecting a first event that signals a beginning of the software operation and controlling the software analyzer to begin delivering the first data set to the debugger;

detecting a second event that signals a beginning of the hardware operation and controlling the hardware analyzer to begin delivering the second data set to the debugger; and

selectively storing together, in order, elements of the first data set and elements of the second data set, where the order is based, at least in part, on the time at which an event associated with generating an element occurred,

where the software component comprises a device driver and the first event comprises an I/O request packet (IRP) arriving at a pre-determined, configurable level in the device driver.

20. (Currently Amended) ~~The method of claim 14,~~

A method, comprising:

establishing a relationship in a debugger between a hardware device and a software component that will perform a software operation related to the hardware device;

configuring a software analyzer to collect a first data set related to the software component as the software component performs the software operation and to cause the first data set to be delivered to the debugger;

configuring a hardware analyzer to collect a second data set related to the hardware device as the hardware device performs a hardware operation and to cause the second data set to be delivered to the debugger;

detecting a first event that signals a beginning of the software operation and controlling the software analyzer to begin delivering the first data set to the debugger;

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detecting a second event that signals a beginning of the hardware operation and controlling the hardware analyzer to begin delivering the second data set to the debugger; and selectively storing together, in order, elements of the first data set and elements of the second data set, where the order is based, at least in part, on the time at which an event associated with generating an element occurred,

where the second event comprises a state change on an operable connection between the hardware device and the software component.

21. (Original) The method of claim 14, where selectively storing together elements of the first data set and elements of the second data set includes selectively adding an element of the second data set to the first data set.

22. (Original) A computer-readable medium storing processor executable instructions operable to perform a method, the method comprising:

establishing a relationship in a debugger between a hardware device and a software component that will perform a software operation related to the hardware device by:

identifying a hardware number known to the software component;

communicating the hardware number to the hardware analyzer;

correlating the software component and a hardware device based on the hardware number; and

configuring the hardware analyzer to analyze the hardware device;

configuring a software analyzer to collect a first data set as the software component performs the software operation and to deliver the first data set to the debugger, where configuring the software analyzer includes one or more of, identifying one or more types of data available in the software component to be reported on by the software analyzer, and establishing a frequency with which the one or more types of data will be sampled;

configuring a hardware analyzer to collect a second data set related to the hardware device as the hardware device performs a hardware operation and to deliver the second data set to the debugger, where configuring the hardware analyzer includes one or more of, identifying one or more types of data available in the hardware device to be reported on by

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the hardware analyzer, and identifying one or more types of events from the hardware device to be reported on by the hardware analyzer;

detecting a first event that signals the beginning of the software operation and controlling the software analyzer to begin delivering the first data set to the debugger, where the software component comprises a device driver and the first event comprises an I/O request packet arriving at a pre-determined, configurable level in the device driver;

detecting a second event that signals the beginning of the hardware operation and controlling the hardware analyzer to begin delivering the second data set to the debugger, where the second event comprises a state change on an operable connection between the hardware device and the software component; and

selectively storing the first data set and the second data set together, in order, where the order is based, at least in part, on the time at which an event associated with generating a member of the first data set or a member of the second data set occurred.

23. (Original) A method, comprising:

engaging a hardware analyzer to analyze a piece of computer hardware;

engaging a software analyzer to analyze a piece of computer software that will service interrupts for the piece of computer hardware;

binding the hardware analyzer to the software analyzer to facilitate storing data received from the hardware analyzer and the software analyzer together, in order, based on time of occurrence;

receiving an event that indicates that data storage should begin; and

storing data received from the hardware analyzer and the software analyzer together, in order, based on time of occurrence.

24. (Currently Amended) ~~The method of claim 23,~~

A method, comprising:

engaging a hardware analyzer to analyze a piece of computer hardware;

engaging a software analyzer to analyze a piece of computer software that will service interrupts for the piece of computer hardware;

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binding the hardware analyzer to the software analyzer to facilitate storing data received from the hardware analyzer and the software analyzer together, in order, based on time of occurrence;

receiving an event that indicates that data storage should begin; and

storing data received from the hardware analyzer and the software analyzer together, in order, based on time of occurrence,

where binding the hardware analyzer to the software analyzer includes programming the hardware analyzer to analyze a piece of computer hardware identified by a hardware number in an I/O request packet (IRP) available to the piece of software.

25. (Original) The method of claim 23, where binding the hardware analyzer to the software analyzer includes establishing a logic connection in a correlating debugger configured to receive data from the hardware analyzer and the software analyzer.

26. (Original) The method of claim 23, where binding the hardware analyzer to the software analyzer includes establishing a physical connection at a correlating debugger configured to receive data from the hardware analyzer and the software analyzer.

27. (Cancelled)

28. (Cancelled)

29. (Original) A set of application programming interfaces embodied on a computer-readable medium for execution by a computer component in conjunction with ordering debug information, comprising:

a first interface for communicating data associated with a hardware analyzer or a hardware device being analyzed by the hardware analyzer;

a second interface for communicating data associated with a software debugger or a software component being analyzed by the software debugger; and

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a third interface for communicating data that facilitates binding the software debugger or the software component with the hardware analyzer or the hardware device to facilitate ordering debug information produced by the hardware analyzer and the software analyzer.

30. (Original) A system for correlating debug data, comprising:

a first logic configured to receive a hardware related debug data from a hardware analyzer;

a second logic configured to receive a software related debug data from a software analyzer;

means for establishing a relationship between the hardware analyzer and the software analyzer to facilitate correlating data received by the first logic and data received by the second logic into a time-ordered set of data.